CERTIFICATE OF EXPRESS MAILING

I hereby certify that this transmittal is being deposited with the U.S. Postal Service, Express Mail No. EV 620180722 US, in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on this 22 day of February, 2005 .

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Cranford, Jr. et al	)	Examiner: T. J. Cleary
Serial No. 09/996,091	)	Art Unit: 2111
Filed: November 28, 2001	)	Confirmation No. 2524
For: **ARCHITECTURE FOR ADVANCED SERIAL LINK BETWEEN TWO CARDS**	)	

Docket No.: RAL920010004US2 (IRA-10-5609)

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on December 28, 2004.

Note: "The applicant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CVF 1.192(a) [emphasis added].

2. **STATUS OF APPLICATION**

This application is on behalf of

☒ other than a small entity

☐ small entity

Verified statement:

☐ attached

☐ already filed

3. **FEE FOR FILING APPEAL BRIEF**

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐	small entity	$ 250.00
☒	other than small entity	$ 500.00

Appeal Brief fee due: $500.00

4. **EXTENSION OF TERM**

Note: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent application. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 27 CFR 1.136 apply.

(complete (a) or (b) as applicable)

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

	Extension Months	Fee for other than small entity	Fee for small entity
☐	one month	$120.00	$60.00
☐	two months	$450.00	$225.00
☐	three months	$1,020.00	$510.00
☐	four months	$1,590.00	$795.00
		Fee:	

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. **TOTAL FEE DUE**

The total fee due is:

Appeal Brief fee	$500.00
Extension fee (if any)	$ 0.00

TOTAL FEE DUE: $500.00

6. **FEE PAYMENT**

☐ Attached is a check in the sum of $_____

☒ Charge **Account No. 50-0563** in the sum of **$500.00.** A duplicate of this transmittal is attached.

7. **FEE DEFICIENCY**

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. if the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge **Account No. 50-0563**.

AND/OR

☒ If any additional fee for claims is required, charge **Account No. 50-0563.**

Respectfully submitted,

Date: 2-21-05

William N. Hogg, Reg. No. 20,156
CUSTOMER NO. 26675

Attachment

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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
A'exandria, VA 22313-1450

Dear Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-entitled application is International Business Machines Corporation of Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

The undersigned attorney is not aware of any related appeals or interferences which would directly affect, or be directly affected by, or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 1-20, as amended, are presently in the application. All 20 claims have been finally rejected.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

The present invention comprises a global architecture for a serial link connection between two cards 12a, 12b which must transmit data across wired media 20. The architecture comprises a transmitter 16 and a receiver 18. The transmitter includes circuitry and a structure to take digital bits from a bit register 24, such as for example, an eight-bit register or a ten-bit register, preferably to at least one latch 28a, 28b, preferably two bits at a time, to an additional latch 32 and convert these bits into serial analog transmission to the receiver 18. A clock (Figure 2) is used. The receiver 18 includes a structure and circuitry (Figure 3) to sample edges of the data on analog transmission of the original digital bits and reconvert the analog serial signal of the digital bits to the original digital bits and store them in a register 68 comparable to the data stored in the original register 24 from which they were selected. Circuitry, including a phase rotator 54, is used to convert an asynchronous signal to a synchronous digital parallel data in conjunction with edge detection.

VI. ISSUES

1. Are claims 1, 2, 5, 6, 9, 10, 11, 12 15, 16, 19 and 20 unpatentable under 35 U.S.C. § 103 (a) over European Patent Application Number 0 686 920 to Jeong et al (hereinafter Jeong), The Microsoft Press Computer Dictionary 3rd Edition (hereinafter Microsoft), and US Patent 6,463,266 to Shohara (hereinafter Shohara)?

2. Are claims 3, 4, 13, and 14 unpatentable under 35 U.S.C. § 103 (a) over Jeong, and Microsoft further in view of US Patent 6,222,380 to Gerowitz et al (hereinafter Gerowitz)?

3. Is claim 7 unpatentable under 35 U.S.C. § 103 (a) over Jeong, Microsoft, and Gerowitz in view of US Patent 5,202,979 to Hillis et al (hereinafter Hillis)?

4. Are claims 8 and 18 unpatentable under 35 U.S.C. § 103 (a) over Jeong, Microsoft, Gerowitz, and Hillis, in view of Newton's Telecom Dictionary, 8th Edition (hereinafter Newton)?

5. Is claim 17 unpatentable under 35 U.S.C. § 103 (a) over Jeong, Microsoft, and Shohara, in view of Hillis?

VII. GROUPING OF THE CLAIMS

(Group 1) Claims 1, 5, 6, 9, 10, 11, 15, 16, 19, and 20 stand or fall together, and claim 11 is representative.

(Group 2) Claims 2 and 12 stand or fall together, and claim 12 is representative.

(Group 3) Claims 3, 4, 13, and 14 stand or fall together, and claim 13 is representative.

(Group 4) Claim 7 stands or falls alone.

(Group 5) Claim 17 stands or falls alone.

(Group 6) Claims 8 and 18 stand or fall together, and claim 18 is representative.

VIII. ARGUMENTS

It should be noted that claims 1-10 are in method form, and claims 11-20 have essentially the same limitations, but are in structure form. In selecting a representative claim for each group, the structure form has been chosen, when applicable.

In Group 1 of the claims, claim 11 has been rejected under 35 U.S.C. § 103 (a) as unpatentable over Jeong, Microsoft, and Shohara. Claim 11 specifically recites "...said circuitry to restore said asynchronous signal to said synchronous data, including a phase rotator to act in conjunction with the circuitry to detect both edges." Shohara teaches the use of a phase rotator to phase shift complex I, Q signals to modulate quadrature (column 9, lines 41-50, and column10, lines 13-19) which is a perfectly valid use of a phase rotator to phase shift complex I, Q signals. However, there is nothing in Shohara to teach or suggest the use of a phase rotator for edge detection as claimed in claim 11. The examiner has taken the position that "It is noted that the features upon which Applicant relies (i.e., the phase rotator performing edge detection) are not recited in the rejected claims." This position is not understood since the claims clearly recite that the phase rotator, in conjunction with the circuitry, performs the edge detection. Appellants never stated or implied that the phase rotator *solely and without collaboration* performed edge detection. What appellants are saying is the phase rotator of Shohara does not alone, or in combination with any circuitry, contribute to edge detection, and appellants have claimed such.

It is not enough that one may modify a reference in view of a second reference, but rather it is required that the second reference suggest modification of the first reference and not merely provide the capability of modifying the first reference.

The CAFC stated In re Piasecki, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984) the following:

"The Supreme Court in Graham v. John Deere Co., 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103". Citing In re Warner, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967)."

The law is quite clear that in order for a claimed invention to be rejected on obviousness, the prior art must suggest the modifications sought to be patented; In re Gordon, 221 U.S.P.Q. 1125, 1127 (CAFC 1984); ACS Hospital System, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (CAFC 1984). The foregoing principle of law has been followed in Aqua-Aerobic Systems, Inc. v. Richards of Rockford, Inc., 1 U.S.P.Q. 2d, 1945 (D.C. Illinois 1986). In the Aqua-Aerobic's case, the Court stated that the fact that a prior reference can be modified to show the claimed invention does not make the modification obvious unless the prior reference suggests the desirability of the modification. The CAFC in the case of In re Gorman, 18 U.S.P.Q. 2d (CAFC 1991) held at page 1888:

"When it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation in the prior art to make the selection made by the applicant [citation]. 'Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination [citations]. . ..

The references themselves must provide some teaching whereby the applicant's combination would have been obvious."

Further, the CAFC, in In re Oetiker, 24 U.S.P.Q. 2nd 1443, 1445 (CAFC 1992) held:

There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself.

Most significantly, the CAFC in the recent case of In re Dembiczak, 50 U.S.P.Q.2nd 1614 (CAFC 1999) held at 1617:

...(examiner can satisfy burden of obviousness in light of combination 'only by showing some objective teaching [leading to the combination]');

Thus, it is clear that where an individual reference does not teach the entire invention, then the modification which the invention represents must be suggested and motivated by some other reference through some objective teaching and cannot come from the application itself, which is not the case here.

There is no suggestion in Shohara as to the use of a phase rotator in any way, alone or in conjunction with circuitry for edge detection. Thus, claim 11, which claims an edge detector in combination with circuitry detects edges, is clearly not taught nor suggested by any reasonable combination of the prior art. Hence, claim 11 is clearly allowable. As indicated, supra, claim 1 is the method analog of claim 1 and claims 5, 6, 9, 10, 15, 16, 19, and 20 are dependent upon claims 1 or 11 and, for the same reasons, are allowable.

Claim 12 is dependent upon claim 11 and, for the same reasons, is allowable. Additionally, claim 12 requires a single bit latch and circuitry to read the digital parallel data out of the first data register to the single bit latch. The locations cited by the examiner to Jeong (Figure 6 and page 6, lines 22-31) do not show a single bit latch to read out the digital parallel data. Latch 118 receives parallel data from latch 117, but latch 118 appears to be a multiple data latch, certainly not a single bit latch. Claim 2 is the method analog of claim 12 and, for this additional reason, both of these claims are allowable over any reasonable combination of the prior art.

Claim 13 has been rejected under 35 U.S.C. § 103 (a) as being unpatentable over Jeong, Microsoft, and Gerowitz. Claim 13 is dependent on claim11 and, for the same reasons, is believed to be allowable since Gerowitz does not overcome the deficiencies of Jeong and Microsoft, and there is no teaching in Gerowitz of a phase rotator for any reason. Additionally, claim 13 requires first, second and third single data bit registers. Gerowitz teaches, in Figure 2,

reading four parallel bits from bit latches L1-L4 into a single bit latch L5. This is not what is claimed, so, for this additional reason, claim 13 is allowable over any reasonable combination of the prior art. Claim 3 is the method analog of claim 13, and claims 4 and 14 are dependent upon claims 3 and 13, and, hence, are allowable.

Claim 7 has been rejected under 35 U.S.C. § 103 (a) as being unpatentable over Jeong, Microsoft, Gerowitz, and Hillis. First, claim 7 is dependent upon claim 1, and requires a phase rotator in combination with circuitry for edge detection. None of the four cited references teaches a phase rotator for any reason and, thus, for this reason, claim 7 is clearly allowable. Additionally, claim 7 requires that the analog signal be converted in the receiver to two one-bit signals, delivered to a shift register, and then stored in a second data register. While there is some disclosure of two bits at a time being sequenced, there is nothing to compare to the specific method claimed in claim 7. Thus, claim 7 is clearly allowable over any reasonable combination of the prior art.

Claim 17 is dependent upon claim 11 and, for the same reasons, is allowable. The addition of Hollis does not render the claim patentable for the reasons stated with respect to claim 7.

Claim 18 is dependent upon claim 11 and, for the same reasons, is believed to be allowable. Additionally, merely citing a dictionary definition does not enable one to determine how data bits should be delivered from a shift register to the second data register. As pointed out above, there has to be a teaching, not the mere possibility of adapting a reference. Thus, claim 18 and its method analog claim 8 are clearly allowable for this additional reason.

SUMMARY

In view of the above, it is believed that each of the claims is allowable over the prior art; thus, the board is respectfully requested to reverse the examiner, and allow the claims.

Respectfully submitted,

Date: 2-21-05

William N. Hogg (Reg. No. 20,156)
DRIGGS, LUCAS, BRUBAKER & HOGG CO., L.P.A.
CUSTOMER NO. 26675

WNH:cg

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APPENDIX

1. A method of transferring stored digital parallel data of multiple bits of data stored in a first data register from a transmitter to a receiver over a hard wired conductor comprising the steps of:

synchronously converting said stored digital data to a serial analog data signal in said transmitter;

transmitting said serial analog signal asynchronously over said hard wired conductor to said receiver; and

restoring said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial analog signal for conversion to parallel data bits and using a phase rotator to convert said asynchronous signal to said synchronous digital parallel data in conjunction with said edge detection.

2. The invention as defined in claim 1 wherein the digital parallel data is read out of said first data register to at least one single bit latch.

3. The invention as defined in claim 2 wherein the data is read out from said first register in said transmitter two bits at a time, each data bit to first and second single data bit registers, and from each first and second single bit data register to a third single bit data register, clocking additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register.

4. The invention as defined in claim 3 wherein the bits from the third single bit register are converted to a single analog serial signal of the data.

5. The invention as defined in claim 1 wherein the data in said first register is comprised of either eight or ten bits.

6. The invention as defined in claim 1 wherein a clocking signal is used to convert said analog serial signal to a digital signal.

7. The invention as defined in claim 3 wherein said analog signal is converted in said receiver to two one-bit signals and delivered to a shift register and then stored in a second data register.

8. The invention as defined in claim 7 wherein said bits in the shift register are delivered synchronously from said shift register to said second data register.

9. The invention as defined in claim 1 wherein said edges are derived from multiple samples.

10. The invention as defined in claim 9 wherein said multiple samples are used to determine the approximate center of said resulting data bit.

11. A structure for transferring stored digital parallel data of multiple bits of data stored in a first data register, comprising a transmitter and a receiver connected by a hard wired conductor;

circuitry to synchronously convert said stored digital data to a serial analog data signal in said transmitter;

circuitry to transmit said serial analog signal asynchronously over said hard wired conductor to said receiver; and

circuitry to restore said asynchronous serial analog signal to synchronous digital parallel data in said receiver corresponding to the data stored in said first data register in said transmitter, including detecting both edges of the data in said asynchronous serial analog signal for conversion to parallel data bits, said circuitry to restore said asynchronous signal to said synchronous digital data, including a phase rotator to act in conjunction with the circuitry to detect both edges.

12. The invention as defined in claim 11 including at least one single bit latch and circuitry to read the digital parallel data out of said first data register to said at least one single bit latch.

13. The invention as defined in claim 12 including first, second and third single data bit registers, and wherein the data is read out from said first register in said transmitter two bits at a time, each data bit to either said first or second single data bit registers, and then from each first and second single bit data register to said third single bit data register, clocking to clock

additional two data bits to be subsequently written to said first and second one bit registers and to said third single bit data register until all bits of the data have been read from the first register.

14. The invention as defined in claim 13 including circuitry to convert the bits from the third single bit register into a single analog serial signal of the data.

15. The invention as defined in claim 11 wherein the data in said first register is comprised of either eight or ten bits.

16. The invention as defined in claim 11 including a clocking signal to convert said analog serial signal to a digital signal.

17. The invention as defined in claim 11 including a second data bit register and circuitry in said receiver to convert said analog signal to two one-bit signals delivered to a shift register, and store the converted bits in said second data register.

18. The invention as defined in claim 17 wherein said bits in the shift register are delivered synchronously from said shift register to said second data register.

19. The invention as defined in claim 11 including circuitry to derive said edges from multiple samples.

20. The invention as defined in claim 19 wherein said circuitry to derive said edges from said multiple samples determines the approximate center of said resulting data bit.